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㉖ Configurable logic array.

㉗ A special interconnect circuit which connects adjacent configurable logic elements (CLEs) in a configurable logic array (CLA) without using the general interconnect structure of the CLA. In one embodiment, an array of CLEs is arranged in rows and columns and a special vertical lead circuit is provided which connects an output lead of a given CLE in a given column to a selected input lead of the CLE above it and below in the same column. Special horizontal lead circuits are provided which connect a given output lead of a given CLE to a selected adjacent input lead of the CLE in the same row.

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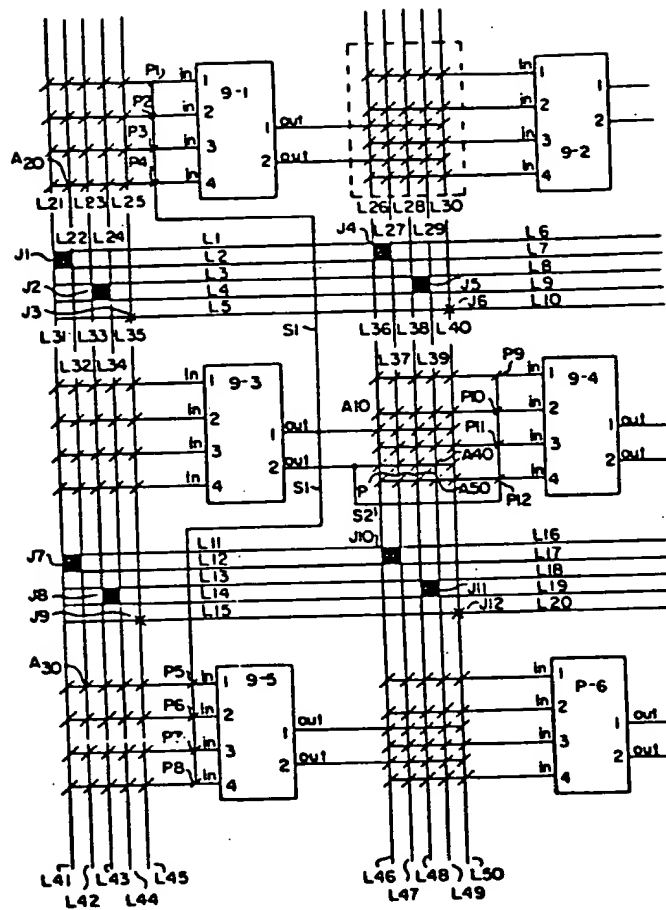


FIG 10

CONFIGURABLE LOGIC ARRAY
DESCRIPTION

This invention relates to a configurable logic array.

5 As explained in detail later, a configurable logic element (CLE) also referred to herein as a logic element, is a combination of devices which are capable of being electrically interconnected by switches operated in response to control bits to form any one of a plurality
10 of logical functions.

Each CLE can include all the circuit elements necessary to provide one or more of the functions provided by an AND gate, flip flop, latch, inverter, NOR gate, exclusive OR gate, and combinations of these
15 functions to form more complex functions. The particular function to be carried out by a CLE is determined by control signals applied to the CLE from control logic. Depending on the control signals, the CLE can function as an AND gate, an OR gate, a NOR gate,
20 a NAND gate or an exclusive OR gate or any one of a number of other logic elements without any change in physical structure. The control logic stores and generates control signals which control the configuration of each CLE.

25 The control logic is typically formed integrally with and as part of the integrated circuit chip containing the CLE. However, if desired the control information can be stored and/or generated outside this integrated circuit and transmitted through pins
30 to the CLE.

In general, a given set of control signals is transmitted to one CLE to control the configuration of that CLE. The control logic is thus arranged to provide any one set of a plurality of sets of control
35 bits to each CLE on the chip. The actual set of control bits provided to each CLE integrated circuit chip depends on the function to be carried out by the integrated

circuit chip or by each CLE on the chip. The configuration of each CLE on the chip is determined by the intended function of the total chip and by the intended formation of that CLE as part of the chip.

5 A configurable logic array (CLA) comprises a plurality of CLEs, each having one or more input leads and one or more output leads, a set of access functions for each input lead and for each output lead, and a general interconnect structure. The general
10 interconnect structure comprises a plurality of general interconnect leads and a plurality of general interconnect junctions. The general interconnect structure has the property that for each lead in the general interconnect structure, there is a programming
15 of the general interconnect junctions which connects the given general interconnect leads to one or more other general interconnect leads by means of a general interconnect junction. An access junction is a programmable junction for connecting a general
20 interconnect lead to an input lead of a CLE or for connecting an output lead of the CLE to a general interconnect lead.

A CLA has the property that there is always a programming of the junctions (both access and general
25 interconnect) so that a given output lead of a given CLE within the CLA can be connected to a given input lead of any other CLE within the CLA.

The junctions in the general interconnect structure and the access junctions are programmed by control
30 signals generated by the control logic described above. A selection of control signals to configure each CLE in a CLA together with a selection of control signals to configure the access functions and the junctions of the general interconnect structure results in one
35 configuration of the CLA.

This invention accordingly provides special

interconnect circuitry which connects selected CLEs in a CLA without using the general interconnect structure. The invention can thus provide on-chip special programmable interconnection circuits between selected adjacent configurable logic elements in a configurable logic array (CLA). In one embodiment for a CLA containing at least a first, a second, a third and a fourth CLE, a special interconnection circuit is provided which permits an output signal on a first output lead of the second CLE to be connected to a selected input lead of the first and third CLE and permits an output signal on a second output lead of the second CLE to be connected to a selected input lead in the fourth CLE. Typically the first and third CLE are in the same column as the second CLE and the fourth CLE is in the same row as the second CLE.

The use of the special interconnect circuits of the invention reduces the use of the general interconnect structure. The reduction in the utilization of the general interconnect structures is so substantial that in many embodiments the number of general interconnect leads and the number of general interconnect junctions is reduced, thus reducing die size.

Frequently, when interconnecting logic elements in a configurable logic array, the access junctions and the junctions of the general interconnect structure are programmed so that the output of one logic element is connected to only one or two other logic elements. If the logic elements that are interconnected are physically close together (and they typically will be placed that way to facilitate interconnecting), the present invention allows a significant amount of general interconnect structure to be eliminated, that is, the special interconnect so reduces the utilization of the general interconnect structure that the overall amount of general interconnect structure provided may be reduced,

thus reducing die size. Also, the speed of signals through this special interconnect will be improved since the number of junctions and the amount of capacitance on the path will be reduced. This type of interconnect is particularly useful when implementing MSI type functions, e.g., shift registers and counters, where adjacent logic elements must be interconnected.

This invention is further described below, by way of illustration, with reference to the accompanying drawings, in which:

Figure 1 illustrates some of the various logic functions capable of being implemented in each logic element in a configurable logic array;

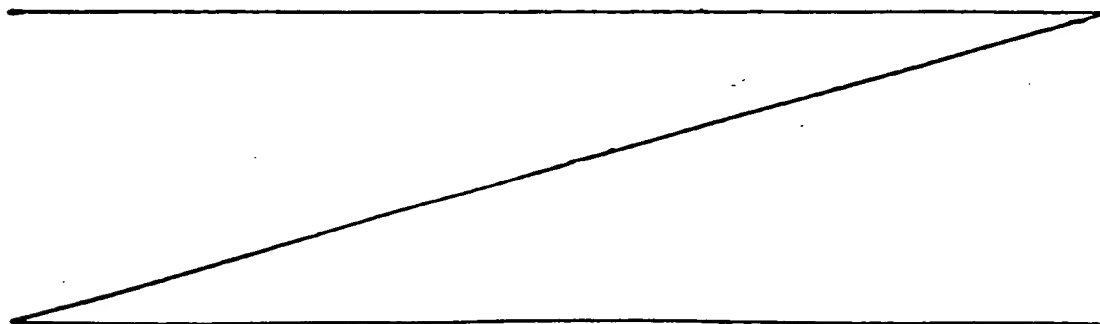
Figure 2 illustrates the internal logic structure of one possible configurable logic element capable of implementing a number of useful functions of two variables A and B;

Figure 3A illustrates a 16 bit RAM circuit wherein any one of sixteen possible input states is capable of being identified and 2^{16} functions are capable of being implemented;

Figure 3B illustrates a selection structure for selecting any one of sixteen bits capable of implementing 2^{16} functions, for transmittal to an output lead;

Figure 3C illustrates one possible Karnaugh map for the structure of Figure 3A;

Figure 3D illustrates the logic gates represented by placing a binary one in the Karnaugh map of Figure 3C at



1 the intersections of the first and second rows and the
2 first column.

3 Figure 4A illustrates a plurality of configurable
4 logic elements (shown as nine logic elements) formed on
5 an integrated circuit chip together with programmable
6 interconnects formed between selected leads to yield
7 desired logic functions and with selected input/output
8 pads and interconnections of the leads between logic
9 elements;

10 Figure 4B shows the key to the cross-connections
11 between crossing conductive leads in Figure 4A;

12 Figure 5 represents a portion of the circuitry of a
13 novel combination static and dynamic shift register
14 appropriate for use with the configurable logic array of
15 this invention;

16 Figures 6A through 6H represent wave forms of use in
17 explaining the operation of the structure of Figure 5;

18 Figure 7A represents a schematic diagram of a con-
19 figurable logic array showing nine of N configurable
20 logic elements where N is a selected integer greater than
21 9 and selected interconnections between conductive leads;

22 Figures 7B-1 through 7B-7 form the key showing the
23 types of interconnections made by the symbols shown in
24 Figure 7A;

25 Figures 8A through 8G illustrate various topologies
26 for forming interconnections between two or more leads of
27 a configurable logic array;

28 Figure 9 shows a configurable logic array without
29 the special interconnect circuit of this invention;

30 Figure 10 shows the configurable logic array of
31 Figure 9 with the special interconnect circuit of this
32 invention; and

33 Figure 11 lists the pass transistor connecting
34 lead A with lead B in Figure 8B.

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U.S. Application No. 588,478, filed 12 March 1984, on an invention of Ross H. Freeman entitled "Configurable Logic Array" is incorporated herein by reference.

It is necessary to explain the configurable logic
 5 elements and general interconnect structure of the configurable logic array described in the above copending application in order to explain the special interconnect structure of the present invention.

Figure 1 illustrates certain logic functions capable
 10 of being implemented by a configurable logic element. The 28 functions shown in Figure 1 are merely illustrative and other elements not shown can, if desired, be implemented by a configurable logic element. The following functions are shown:

15	<u>Element</u>	<u>Function</u>
	1	AND gate
	2	NAND gate
	3	AND gate with inverted input
	4	NAND gate with inverted input
20	5	OR gate
	6	NOR gate
	7	exclusive OR gate
	8	exclusive NOR gate
	9	3 input AND gate
25	10	3 input NAND gate
	11	3 input OR gate
	12	3 input NOR gate
	13	OR gate with one input comprising AND gate
	14	NOR gate with one input comprising AND gate
30	15	AND gate with one input comprising OR gate
	16	NAND gate with one input comprising OR gate
	17	3 input AND gate with one input inverted

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1	18	3 input NAND gate with one inverted input
2	19	3 input OR gate with one inverted input
3	20	3 lead NOR gate with one inverted input
4	21	one of two inputs multiplexer
5	22	inverting one of two inputs multiplexer
6	23	"D" flip flop with reset
7	24	Set-Reset latch
8	25	"D" flip-flop with reset and inverted
9		output
10	26	Set-reset latch with reset and inverted
11		output
12	27	"D" flip-flop with set
13	28	"D" flip-flop with set and inverted output

14
15 Of course, other logic functions can also be imple-
16 mented in a configurable logic element.

17 Figure 2 illustrates the internal logic structure of
18 one possible configurable logic element which is capable
19 of implementing all useful basic functions of the two
20 variables A and B, with the functions being selected by
21 configuration control signals C_0 , \bar{C}_0 , C_1 , \bar{C}_1 , ... through
22 C_5 on control leads C_0 , \bar{C}_0 , ... through C_5 . In this
23 example each control lead is connected to the gate of an
24 N channel enhancement mode pass transistor. To implement
25 an AND gate function using the structure shown in Figure 2,
26 the input leads labeled A and B are shunted past invert-
27 ers 21 and 22, respectively, to AND gate 25 by high level
28 signals on the C_1 and C_0 configuration control leads
29 which, being connected to the gates of N channel enhance-
30 ment mode pass transistors 29c and 29d, cause pass tran-
31 sistors 29c and 29d to turn on.

32 Low level signals are applied to the configuration
33 control leads \bar{C}_0 and \bar{C}_1 , thus blocking the output signals
34 of inverters 21 and 22 from AND gate 25. In addition, a
35 high level signal on lead C_5 is applied to enable AND
36 gate 25. Thus three input AND gate 25 functions as a
37 two-input AND gate with respect to the signals A and B.
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1 The output signal of AND gate 25 provides one input
2 signal to NOR gate 26. A second input signal to NOR gate
3 26 is provided by the output signal of AND gate 24. The
4 output signal of AND gate 24 is held at a logical 0 by
5 applying a logical 0 to configuration control lead C4.
6 Thus the control signals C2 and C3 are "don't cares",
7 that is, these signals can be high or low without affect-
8 ing the output signal of AND gate 24. Since the output
9 signal of AND gate 24 is a logical 0, and since the
10 tristate control input signal to NOR gate 26 is a logi-
11 cal 0, it is easy to see that AND gate 25, AND gate 24
12 and NOR gate 26 function together as a NAND gate with
13 respect to input signals A and B. Since the tri-state
14 control signal input to NOR gate 27 is a logical 0 (except
15 during reset), NOR gate 27 serves as an inverter with
16 respect to the output signal of NOR gate 26. The output
17 signal of NOR gate 26 is applied to the gate of N channel
18 transistor 29a (the source of which is grounded and the
19 drain of which is connected to output lead 2) and the
20 complement of the output signal of NOR gate 26 is applied
21 to the gate of N channel transistor 29b (the source of
22 which is connected to a power supply and the drain of
23 which is connected to both the output lead 28 and the
24 drain of N channel transistor 29a). Thus, transistors
25 29a and 29b function as an inverter with respect to the
26 output signal of NOR gate 26. Thus, the structure of
27 Figure 2 configured as described above performs the
28 function of an AND gate with respect to the signals A and
29 B. Other logic functions can also be produced by appro-
30 priate selection of the control signals to be supplied to
31 the configuration control leads C0 through C5 to activate
32 the appropriate pass transistors and gates within the
33 structure.

34 Figure 3A illustrates a 16 bit RAM capable of produc-
35 ing an output signal in response to any one of sixteen
36 possible combinations of input signals. Thus input
37 signals A and B control the X decoder to select any one
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1 of the four columns in the 16 bit RAM. Input signals C
2 and D control the Y decoder to select any one of the four
3 rows in the 16 bit RAM. The 16 bit RAM produces an
4 output signal representative of the bit at the intersec-
5 tion of the selected row and column. There are 16 such
6 intersections and thus sixteen such bits. There are 2^{16}
7 possible combinations of functions capable of being
8 represented by 16 bits. Thus, if a NOR gate is to be
9 simulated by the 16 bits in the RAM, the Karnough map for
10 the RAM would be as shown in Figure 3C. In Figure 3C all
11 bits are "0" except the bit at the intersection of the
12 first row (representing A=0, B=0) and the first column
13 (representing C=0, D=0). Should a less frequently used
14 function be desired to be generated by the 16 bit RAM,
15 (for example, should a "1" output signal be desired for
16 A=1, B=0, C=0 and D=0) then a binary "1" is stored at the
17 intersection of the second row and the first column.
18 Should a binary "1" be desired both when A=0, B=0, C=0
19 and D=0 and also when A=1, B=0, C=0 and D=0, then a
20 binary "1" is stored at each of the intersections of the
21 first column with the first row and the second row. The
22 logic circuit represented by this loading of the RAM is
23 as shown in Figure 3D. Thus the RAM of Figure 3A repre-
24 sents an elegant and simple implementation of any one of
25 2^{16} logic functions.

26 Figure 3B shows another structure for yielding any
27 one of sixteen select bits. Each of registers 0-15 in
28 the vertical column to the left labeled "16 Select Bits",
29 contains a selected signal, either a binary 1 or 0. By
30 selecting the proper combination of A, B, C, and D, a
31 particular bit stored in a particular one of the sixteen
32 locations in the 16 Select Bits register is transmitted
33 to the output lead. Thus, for example, to transmit the
34 bit in the "1" register to the output lead, the signal A,
35 B, C, D is applied to the leads so labeled. To transmit
36 the signal labeled "15" in the sixteenth location in the
37 16 Select Bits register to the output lead, the signal A,
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1 \bar{B} , \bar{C} , and \bar{D} is applied to the appropriate columns.
2 Again, any one of 2^{16} logic functions can be implemented
3 using this structure.

4 Figures 4A illustrates a configurable logic array
5 containing nine configurable logical elements. As shown
6 in Figure 4a, each CLE of the nine CLEs 40-1 through 40-9
7 has a plurality of input leads and one or more output
8 leads. Each input lead has a plurality of access junctions
9 each connecting a selected general interconnect lead to
10 the input lead. The access junctions for input lead 2 of
11 CLE 40-7 are labeled A1 through A4 in Figure 4a. The
12 access junctions for the other input leads are indicated
13 schematically but are not labeled for the sake of clarity.
14 Similarly, each output lead of each CLE has a plurality
15 of access junctions each connecting the output lead to a
16 corresponding one of the general interconnect leads. The
17 access junctions are indicated schematically for each
18 output lead of each CLE in Figure 4a. The access junctions
19 for the output lead of CLE 40-7 are labeled B1 through
20 B5. The leads in Figure 4a which are neither input leads
21 nor output leads are called general interconnect leads
22 and the junctions in Figure 4a which are not access
23 junctions for input and output leads are called general
24 interconnect junctions. As shown in Figure 4A, nine
25 logic elements are placed on an integrated circuit chip
26 together with programmable access junctions and a general
27 interconnect structure which comprises general interconnect
28 leads and programmable general interconnect junctions for
29 connecting various leads to other leads. The general
30 interconnect structure set of general interconnect leads
31 and of programmable junctions interconnecting the general
32 interconnect leads have the property that for each general
33 interconnect lead in the general interconnect structure
34 there is a programming of the general interconnect junctions
35 which connects the given general interconnect lead
36 to one or more other leads in the general interconnect
37 structure. Moreover, there is a programming of the

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1 junctions (both access and general interconnect) such
2 that for any given output lead of any CLE in the CLA, and
3 for any given input lead of any other CLE in the CLA,
4 there is a programming of the junctions such that the
5 given output lead is connected to the given input lead.
6 An electrical path from a given output lead to a given
7 input lead always contains at least two access junctions
8 and at least a portion of a general interconnect lead.
9 For example, one electrical path from the output lead of
10 CLE 40-8 to the second input lead of CLE 40-9 contains
11 access junctions A7 and B7 and the marked portion P of a
12 general interconnect lead. Typically, an electrical path
13 from an output lead of one CLE to an input lead of another
14 CLE will also contain one or more general interconnect
15 junctions. Each of logic elements 40-1 through 40-9
16 represents a collection of circuitry such as that shown
17 in Figure 2 or some similar structure capable of being
18 configured as described above in Figure 2 to perform any
19 one of a number of logic functions. To program the
20 circuitry, (both the configurable interconnect switches
21 and the configurable logic elements), selected signals are
22 applied to input leads identified as configuration control
23 input leads thereby to generate a desired logical function
24 in each of the logic elements and to interconnect the
25 logic elements as desired. In Figure 4A, no specific
26 lead has been identified as an input lead for the configura-
27 tion control signals. However, any particular I/O pad
28 can be selected for this purpose. The configuration
29 control bits can be input into the configurable logic
30 array either in series or in parallel depending upon
31 design considerations where they are typically stored in
32 a programming register (not shown). Alternatively, the
33 configuration control bits may be stored in a memory on
34 chip. In addition, another I/O pad will be used on input
35 clock signals which are used, inter alia, for the loading
36 of the configuration control signals into the programming
37 register. When the configurable logic array shown in
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1 Figure 4A has been configured, selected output signals of
2 logic elements 40-1 through 40-9 are provided to selected
3 I/O pads. Figure 4B illustrates the meaning of the
4 junction symbols used in Figure 4A.

5 To configure a logic element such as logic element
6 40-1 (Figure 4A, 4B) a number of bits must be applied to
7 the configuration control leads such as leads C0 through
8 C5, as shown, for example, in Figure 2. To do this, a
9 shift register, for example, is utilized as part of each
10 configurable logic element. Figure 5 illustrates a shift
11 register which may be used. The shift register of Figure 5
12 is illustrated showing two basic storage cells. Each
13 storage cell is capable of storing one bit of information.
14 Of course, an actual shift register will contain as many
15 storage cells as required to configure the logic element
16 of which the shift register is a part, to its desired
17 configuration. In operation, an input signal is applied
18 to input lead 58. This input signal (shown in Figure 6D)
19 contains bit stream to be stored in the shift register as
20 configuration control bits to configure the configurable
21 logic element to perform a desired logic function or to
22 configure (program) an access junction or a general
23 interconnect junction between general interconnect leads
24 in a manner to be described shortly. Thus the sequence
25 of pulses applied to input lead 58 represents those
26 pulses which when stored in the storage cells of the
27 shift register will activate the configuration control
28 bits in the proper manner to achieve the desired functional
29 and/or interconnection result. For example, if the
30 circuit of Figure 2 is to be configured to form an AND
31 gate, the pulses C0, C1, C2, C3, C4, and C5 would be
32 represented by 1,1,X,X, 0,1.

33 The sequence of pulses applied to input lead 58 is
34 synchronized with clocking pulses $\phi 1$ and $\phi 2$ applied to
35 leads 57 and 59 respectively. Thus in the first period
36 of operation clocking pulse $\phi 1$ goes high (Fig. 6A),
37 clocking pulse $\phi 2$ is low (Fig. 6B), the hold signal
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1 (Fig. 6C) is low during shifting thereby facilitating the
 2 passage of data through sequentially connected cells 5-1,
 3 5-2 et al. of the shift register. To shift the pattern
 4 01010 into the shift register, the following operations
 5 occur: The input signal on lead 58 is low during approx-
 6 imately the first half cycle of the clocking period t_1 .
 7 The output signal \bar{Q}_1 of inverter 51-1 goes to a high
 8 level in response to the low level input signal and ϕ_1
 9 high to enable pass transistor 53-1. Some time through
 10 the first clocking period t_1 , the clock signal ϕ_1 goes
 11 low (Fig. 6A) and the clock signal ϕ_2 shortly thereafter
 12 goes high (Fig. 6B) to enable pass transistor 55-1.
 13 Consequently, the high level output signal \bar{Q}_1 is trans-
 14 mitted to the input lead of inverter 52-1 by enabled pass
 15 transistor 55-1 and thereby produces a low level output
 16 signal Q_1 on the output lead of inverter 52-1. Thus at
 17 the end of period t_1 , the output signal Q_1 (Figure 6F)
 18 from inverter 52-1 is low level. The output signals \bar{Q}_2
 19 and Q_2 from inverters 51-2 and 52-2 in the second cell
 20 are still indeterminate because no known signal has yet
 21 propagated to the second storage cell 5-2 to change the
 22 signals of these inverters to a known state.

23 At the beginning of the second period (labeled " t_2 "
 24 in Fig. 6A), ϕ_1 goes high (Fig. 6A) and ϕ_2 is low (Fig.
 25 6B) having gone low before period t_1 ended. The input
 26 signal (Figure 6D) now has risen to a high level repre-
 27 senting a binary 1 and thus the output signal \bar{Q}_1 of
 28 inverter 51-1 has gone low. The output signal Q_1 of
 29 inverter 52-1 remains low because pass transistor 55-1 is
 30 held off by the low level ϕ_2 signal. Some time through
 31 the second period ϕ_1 goes low followed a fraction of time
 32 later by ϕ_2 going high. At this time, the output sig-
 33 nal \bar{Q}_1 is transmitted through pass transistor 55-1 to
 34 inverter 52-1 thereby driving the output signal Q_1 from
 35 inverter 52-1 to high level. Meanwhile, during period t_2
 36 the previous low level signal on Q_1 has driven the output
 37 signal \bar{Q}_2 of inverter 51-2 to a high level when Q_1 was at
 38

1 a high level to enable pass transistor 53-2 and the
2 change in ϕ_2 from a low level to a high level in the
3 second half of period t_2 to enable pass transistor 55-2
4 drives the output signal Q_2 from inverter 52-2 to a low
5 level. In this manner, the input signal on lead 58 (Fig.
6 6D) is transmitted through each of the cells 5-1, 5-2,
7 5-3 et al. in the shift register. Upon the transfer into
8 the shift register of the desired information, the hold
9 signal (Figure 6C) is enabled (i.e., driven to a high
10 level) thereby to connect the feedback leads 50-1, 50-2,
11 and 50-3 et al. from the output leads of inverters 52 to
12 the input leads of inverters 51 so as to hold the infor-
13 mation then in each cell indefinitely. In operation, the
14 signal stored in a given cell, e.g. 5-1, is connected to
15 a configuration control or to an interconnect pass device.

16 The \bar{Q}_1 , Q_1 , \bar{Q}_2 , Q_2 , etc., of the shift register are
17 directly connected to the (configuration) control inputs
18 of a logic element or the pass devices of the general
19 interconnect junctions.

20 When ϕ_1 is low, ϕ_2 and hold may be brought high,
21 thus holding the data indefinitely. The entire shift
22 register may be set or cleared by setting or clearing the
23 input with ϕ_1 and ϕ_2 both high and HOLD low. Enough
24 set/reset time must be allowed for the signal to propagate
25 the entire length of the shift register to clear the
26 shift register in this manner. Naturally this time is
27 dependent upon the length of the shift register.

28 The shift register operates in its dynamic phase by
29 storing the information being shifted as charge on the
30 gates of the transistors (not shown in Figure 5 but
31 well-known) comprising inverters 51-1, 52-1, 51-2, 52-2
32 et al. of the shift register. These inverters are of
33 well-known design and will not be described in detail.
34 The use of dynamic shift register is important because a
35 dynamic shift register uses six transistors and thus

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1 takes up very little area. The dynamic shift register is
2 converted to a static latch by adding only one transistor.
3 Thus the dynamic shift register (static latch) can be
4 easily fabricated as part of a configurable logic element
5 without adding significant complexity to the circuit or
6 consuming significant semiconductor area. Because of the
7 "hold" signal, the dynamic shift register can become a
8 static latch because placing the shift register on hold
9 automatically refreshes the data. Thus a separate refresh
10 circuit is not needed.

11 It is apparent from the above description that the
12 dynamic shift register (static latch) circuit does not
13 need refreshing once it has been latched into a hold
14 position. This is accomplished by use of the feedback
15 circuit comprising lead 50-1 and pass transistor 54-1 in
16 cell 5-1, for example.

17 Figure 7A shows an additional configurable logic
18 array containing a plurality of configurable logic ele-
19 ments. In particular, configurable logic elements 70-1,
20 70-2, 70-4 and 70-5 are shown in their entirety while
21 configurable logic elements 70-3, 70-6 and 70-7 through
22 70-9 are shown partially. In particular, the complete
23 interconnections of these last five logical elements are
24 not shown. The structure shown in Figure 7A is merely
25 illustrative of the types of configurations and connec-
26 tions which can be implemented using the configurable
27 logic array of this invention and does not depict an
28 actual circuit configured to carry out an intended func-
29 tion.

30 As shown in Figure 7A, given leads in the general
31 interconnect structure can be interconnected by various
32 general interconnection junctions. The symbols rep-
33 resenting the interconnect junctions shown in Figure 7A
34 are illustrated in Figure 7B. In particular, while the
35 schematics depicting various interconnect junctions are
36 to some extent self-explanatory, the conventions used in
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1 Figures 7B-1 through 7B-7 are further explained in Figures
2 8A through 8G.

3 Figure 8A is the schematic of a circuit for making a
4 number of different interconnections between four leads
5 coming together at a junction point: horizontal leads
6 90-1 and 90-4 and vertical leads 90-2 and 90-3. Thus,
7 pass transistor 2, when activated into the conducting
8 state, connects lead 90-3 to lead 90-1. Pass transistor 1,
9 when conducting, connects lead 90-3 to lead 90-4. Pass
10 transistor 4, when conducting, connects lead 90-4 to lead
11 90-2 and pass transistor 3, when conducting, connects
12 lead 90-1 to lead 90-2. Pass transistors 5 and 6, when
13 off, separate leads 90-4 from leads 90-1 and separate
14 lead 90-2 from lead 90-3, respectively. Thus, should it
15 be desired to connect vertical lead 90-2 to vertical lead
16 90-3, pass transistor 6 is activated. Likewise, should
17 it be desired to connect horizontal lead 90-1 to horizontal
18 lead 90-4, pass transistor 5 is activated. The terminology
19 used to represent the possible connections between a
20 plurality of leads can become quite complex. Thus, a
21 simplified notation system as shown in Figures 8B to 8D
22 has been adopted.

23 In Figure 8B, a plurality of pass transistors 92-1
24 through 92-13 are shown. The convention adopted in
25 Figure 8B is to have a given pass transistor represented
26 by a single short line. Thus, the line labelled 92-1
27 represents a pass transistor. Pass transistor 92-1 is
28 drawn so that its two ends point to the ends of the leads
29 91-5 and 91-6 being interconnected by pass transistor
30 92-1. Similarly, the right end 93a of pass transistor
31 92-1 is aimed to the end 94a of lead 91-5. The left end
32 93b of pass transistor 92-1 is aimed to the end 94b of
33 lead 91-6. For simplicity and to avoid cluttering the
34 drawing in Figure 8B, the other ends of the transistors
35 are not labelled. However, by visually aligning the line
36 representing a given pass transistor with the ends of the
37 leads 91-1 through 91-6 the particular two leads inter-
38

1 connected by that pass transistor can be determined.
2 Thus, pass transistor 92-7 interconnects horizontal lead
3 91-4 with horizontal lead 91-1. Pass transistor 92-13
4 interconnects horizontal lead 91-4 with horizontal lead
5 91-2. Pass transistor 92-12 interconnects lead 91-3 with
6 lead 91-5. Similar connections can be made between the
7 other pass transistors and the other leads. The table in
8 Figure 11 lists the pass transistor connecting lead A
9 with lead B.

10 The above description assumes that only two leads
11 are to be interconnected. If more than two leads are to
12 be interconnected, the structure of Figure 8B can also be
13 used for this purpose. Thus, lead 91-3 can be connected
14 to lead 91-2 by turning on pass transistor 92-10. Simul-
15 taneously, lead 91-3 can be connected to lead 91-4 by
16 turning on pass transistor 92-13. Alternatively, lead
17 91-3 could be connected to lead 91-4 by turning on pass
18 transistor 92-11. Of course, this would also connect
19 lead 91-4 through lead 91-3 and pass transistor 92-10 to
20 lead 91-2. In addition, lead 91-6, for example, could be
21 connected to the three leads 91-2, 91-3, 91-4 by turning
22 on pass transistor 92-8. The number of interconnections
23 which can be made using this structure is limited only by
24 the imagination of the designer. In the limit, if all
25 the pass transistors are turned on, all the leads 91-1 to
26 91-6 are interconnected. The resulting structure has a
27 large capacitance which can actually be used in circuits
28 as a component. Of course, all leads in Figure 8B can be
29 interconnected by turning on as few as five leads. Note
30 that in Figure 8B leads 91-1 and 91-2 cannot be directly
31 connected to each other nor can lead 91-4 be directly
32 connected to lead 91-5 without involving another lead.
33 However, this omission is not of importance because in
34 general in an integrated circuit there is no need for two
35 horizontal leads to carry the same signal. Of course,
36 two additional pass transistors could be added to the
37 structure of Figure 8B if Figure 8B is considered to be
38

1 merely a symbolic representation of intersecting leads
2 and leads 91-1 and 91-2 are merely shown for convenience
3 as being parallel but in fact represent non-parallel
4 leads on an integrated circuit.

5 Turning to Figure 8C another possible interconnection
6 topology is illustrated. In Figure 8C leads 1 to 8 are
7 shown coming together at a complicated junction. Leads 1
8 and 8 are parallel horizontal to the left, leads 4 and 5
9 are parallel horizontal to the right, leads 2 and 3 are
10 parallel vertical up and leads 6 and 7 are parallel
11 vertical down. Looking for a moment at lead 6, the end
12 6a of lead 6 can be connected sensibly to the ends "a" of
13 leads 1, 2, 3, 4, 5 and 8. It is not sensible to connect
14 lead 6 to lead 7 because theoretically the two leads are
15 going in one direction only one lead is required to carry
16 the necessary information in that direction. Since lead
17 6 has six desirable possible connections and each of the
18 other seven leads also has 6 desirable possible connections
19 there are a total of forty-eight desirable possible
20 connections between the eight leads of Figure 8C. Since
21 a given pass transistor connects two ends, twenty-four
22 pass transistors are required to make the desired forty-
23 eight connections. Each pass transistor has its ends
24 labelled in Figure 8C to illustrate the leads which are
25 connected by a given pass transistor. Thus, pass transis-
26 tor 6-8 interconnects the end 6a of lead 6 to the end 8a
27 of lead 8. Pass transistor 7-5 interconnects the end 7a
28 of lead 7 to the end 5a of lead 5. Because of the com-
29 plexity of the structure of Figure 8D a slightly different
30 convention (a line with numbers on both ends) has been
31 adopted for representing the pass transistor than was
32 described above in conjunction with Figure 8B.

33 Figure 8D illustrates a configuration similar to
34 that of Figure 8C with only twenty interconnection tran-
35 sistors rather than the twenty-four shown for the junction
36 in Figure 8C. As shown in Figure 8D pass transistors
37
38

1 1-6, 7-4, 2-5 and 8-3 have been deleted from the transis-
2 tors shown in Figure 8C.

3 Figure 8E illustrates the direct connections that
4 would be possible if the four pass transistors omitted
5 from Figure 8C were in fact included. (A connection
6 between lead A and lead B is direct if A and B are con-
7 nected by a single pass transistor.) The dashed lines
8 show the direct interconnections possible by these omitted
9 transistors. Figure 8D shows only twenty pass transistors
10 whereas twenty-four pass transistors are necessary to
11 make all possible direct connections. Figure 8F illus-
12 trates, however, the way in which it is possible to
13 interconnect leads 4 and 7 without the four transistor
14 connections shown in Figure 8E being present. Thus, for
15 example, to connect lead 4 to lead 7, lead 4 is connected
16 directly to lead 8 by means of transistor 4-8 while lead
17 8 is connected to lead 7 by pass transistor 8-7.

18 Note that each of the interconnections shown above
19 in Figures 8A through 8E requires only one pass transistor
20 in order to connect one junction lead to another junction
21 lead while for the particular configuration illustrated
22 in Figure 8F two pass transistors are required.

23 Figure 8G illustrates types of possible interconnec-
24 tions. The leads interconnected are illustrated by
25 showing continuous straight line segments meeting. These
26 interconnections are self-explanatory.

27 The symbology used in Figures 7B-1 through 7B-7 is
28 identical to the symbology just explained in conjunction
29 with Figures 8A through 8G. Thus, for example, Figure
30 7B-7 illustrates a solid block involving a twenty pass
31 transistor junction. The twenty transistor interchange
32 shown in Figure 7B-7 corresponds precisely to the inter-
33 change explained in more detail above in conjunction with
34 Figure 8D.

35 Figure 7B-1 illustrates three transistors capable of
36 making a T connection or a crossconnection but not a full
37 interconnection. By full interconnection is meant the
38

1 ability to connect each of the leads (in Figure 7B-1,
2 four leads) coming into a junction to any combination of
3 other leads coming into the junction.

4 Figure 7B-2 shows a one transistor junction to
5 connect a row with a column. Figure 7B-3 shows a six
6 transistor full interconnection wherein any one of four
7 leads coming into a junction can be connected to any one
8 of the other three leads coming into the junction. Fig-
9 ure 7B-4 shows six leads coming into a junction wherein
10 ten pass transistors are used to interconnect any one of
11 the six input leads to any one of the five other leads of
12 the junction. Figure 7B-5 illustrates a four-lead junc-
13 tion where two horizontal continuous leads are intercon-
14 nected with two separate vertical leads using five pass
15 transistors.

16 Figure 7B-6 illustrates a three-transistor junction
17 wherein any one of three leads coming into a junction can
18 be interconnected with any one of the other two leads.
19 Figure 7B-7 illustrates the twenty-transistor junction
20 for interconnecting any one of eight input leads to any
21 one of the other eight input leads except that lead
22 parallel and adjacent to the lead being interconnected as
23 illustrated in Figure 8D and except for the four intercon-
24 nections shown in Figure 8E (which also cannot be directly
25 made using the structure of Figure 7B-7).

26 A CMOS transmission gate may be used in place of a
27 pass transistor in implementing the interconnections
28 described above.

29 Frequently, when interconnecting logic elements in a
30 configurable logic array, such as the logic array shown
31 in Figure 4A, which includes configurable logic elements
32 40-1 through 40-9, their input and output leads, their
33 access junctions and the general interconnection leads
34 and various general interconnect junctions, it is desired
35 that the output signal from one configurable logic element
36 be only connected to one or two other configurable logic
37 elements. To facilitate interconnection, as a general
38

1 rule, it is desirable to position the one logic element
2 as close as possible to the other logic element(s) to
3 which it is to be connected.

4 Fig. 9 shows a portion of a configurable logic
5 array, including configurable logic elements 9-1 through
6 9-6 and general interconnection leads L1 through L50,
7 together with general interconnect junctions J1 through
8 J12. The junction symbols in Figure 9 have the same
9 meaning as explained in Figure 4b. One set of 30 access
10 junctions is indicated by the dotted lines in Figure 9.
11 This set includes 10 access junctions for the output
12 leads of CLE 9-1 and 20 access junctions for the four
13 input leads of CLE 9-2. The access junctions are not
14 labeled individually for the sake of clarity. Referring
15 to Figure 9, suppose, for example, that it is desired to
16 connect a signal on output lead 1 of configurable logic
17 element 9-3 to input lead 4 of configurable logic element
18 9-1, and that simultaneously it is desired to connect the
19 output signal on output lead 1 of CLE 9-3 to input lead 1
20 of CLE 9-5. In order for the output signal on output
21 lead 1 of CLE 9-3 to arrive at input lead 4 of CLE 9-1,
22 it would be necessary for the signal to pass through at
23 least four junctions, for example, access junction A10,
24 general interconnect junction J4, general interconnection
25 junction J1 and access junction A20. Similarly, in order
26 to arrive at input lead 1 of CLE 9-5, it would be necessary
27 for the signal on output lead 1 of CLE 9-3 to pass through
28 at least four junctions. For example, access junction
29 10, general interconnect junction J10, general intercon-
30 nection junction J7 and access junction A30. Similarly,
31 if it is desired for the output signal on output lead 2
32 of CLE 9-3 to be connected to input lead 4 of CLE 9-4, it
33 would be necessary for the signal to pass through at
34 least two junctions and at least a portion P of the
35 general interconnect lead L38 between these two junctions.
36 For example, the output signal on lead 2 of CLE 9-3 might
37 pass from output lead 2 via access junction A40 via the
38

1 marked portion P of general interconnect lead 39 to
2 access junction 50 on input lead 4 of CLE 9-4. Thus,
3 even though configurable logic element 9-3 has been
4 positioned in the configurable logic array shown in
5 Figure 9 so that it is next to configurable logic array
6 9-1, 9-5 and 9-4, it is nevertheless necessary for the
7 output signals from CLE 9-3 to pass through several
8 junctions and at least a portion of a general interconnect
9 lead in order to arrive at the proper input lead. This
10 utilization of the general interconnect leads is reduced
11 in one embodiment of the invention by providing each CLE
12 with a special vertical lead which enables one output
13 lead of each configurable logic element to be directly
14 connected to any input lead of the configurable logic
15 element directly above it or below it in the configurable
16 logic and by providing a special horizontal lead circuit
17 which connects the second output of each CLE directly to
18 a selected input lead of the CLE to its immediate right
19 in the configurable logic array. For example, Figure 10
20 shows CLE 9-3 provided with a special vertical lead
21 circuit (SVC) of the present invention which connects
22 output lead 1 selectably to each input lead of CLE 9-1
23 and 9-5 directly above and below CLE 9-3. The SVC circuit
24 includes lead S1 connected to output lead 1 and program-
25 mable access junctions P1, P2, P3, P4 for selectively
26 connecting lead S1 with a desired input lead of CLE 9-1.
27 The SVC also includes programmable access junctions P5,
28 P6, P7 and P8 for selectively connecting lead S1 of
29 CLE 9-3 with a desired input lead of CLE 9-5. Similarly,
30 a special horizontal lead circuit (SHC) includes lead S2
31 connected to output lead 2 of CLE 9-3 and programmable
32 access junctions P9, P10, P11, and P12 for selectively
33 connecting output lead 2 of CLE 9-3 with a desired input
34 lead of CLE 9-4. The access junctions P1 through P12 are
35 only indicated schematically in Figure 10, however, they
36 each may be implemented by a single pass transistor and
37 programmed in the manner described above for the junctions
38

1 of the general interconnect structures. The inclusion of
2 such special interconnect circuitry has at least two
3 advantages: first; it may reduce the overall usage of
4 the general interconnect leads and junctions to the point
5 where some of these leads and junctions may be eliminated
6 from the configurable logic array. This, of course,
7 depends on the interconnection demands of the other CLEs
8 in the CLA. Secondly, the speed of the signals through
9 these special interconnection circuits will be improved
10 since the number of transmission gates or pass transistors
11 and the amount of capacitance on the path will be reduced.
12 Provision of special interconnection circuits is particu-
13 larly useful when implementing MSI type functions, for
14 example, shift registers and counters, where adjacent
15 logic elements must be interconnected.

16 In view of the above description, which is
17 illustrative only, it will be evident to one of ordinary
18 skill in the art that a variety of special inter-
19 connections between adjacent configurable logic elements
20 in a configurable logic array may be provided within the
21 scope of the invention.

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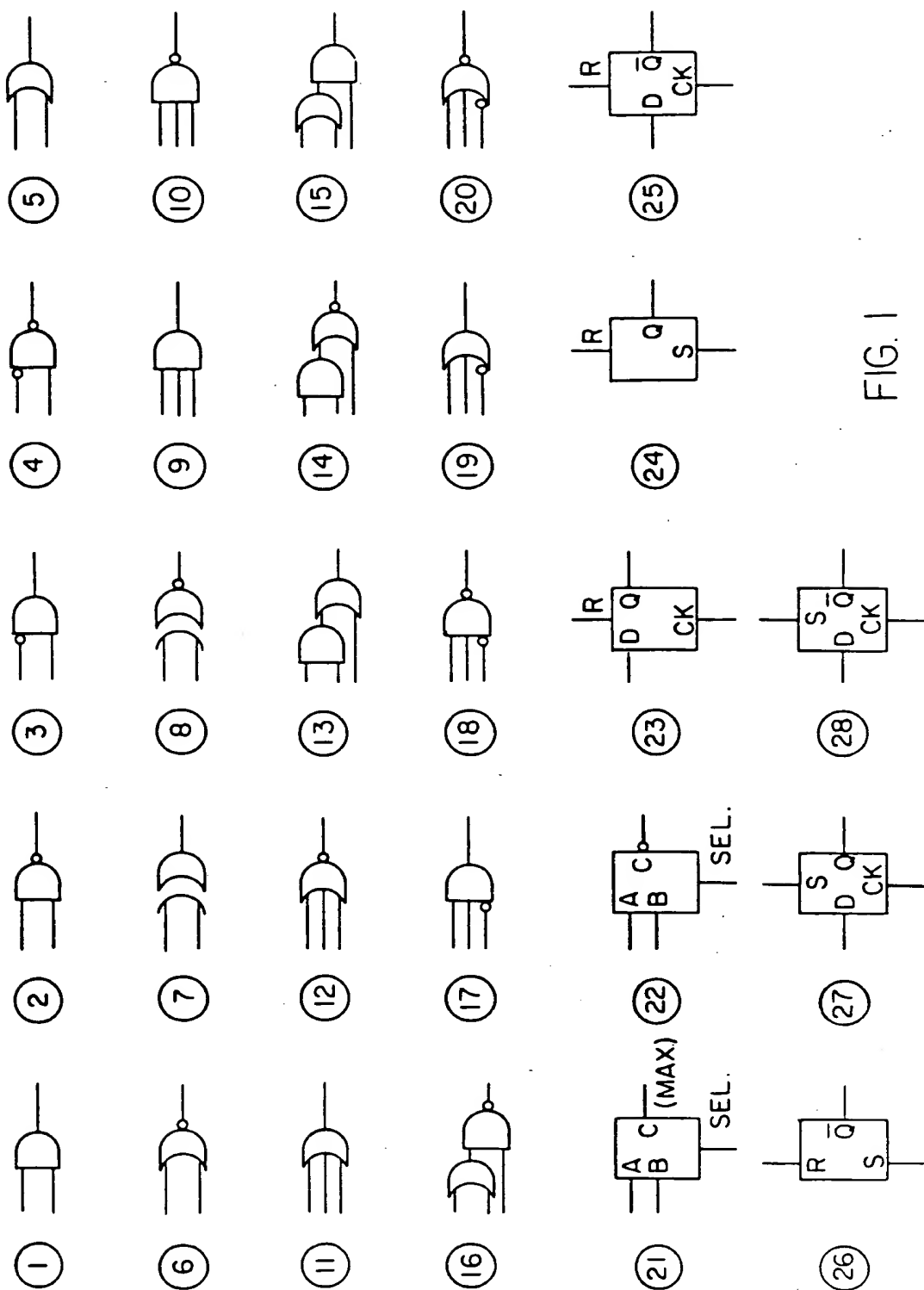
CLAIMS

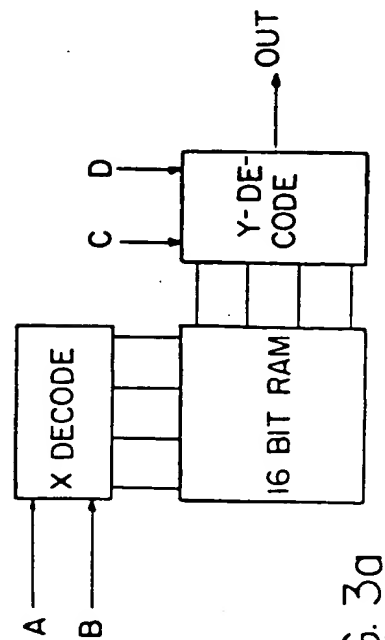
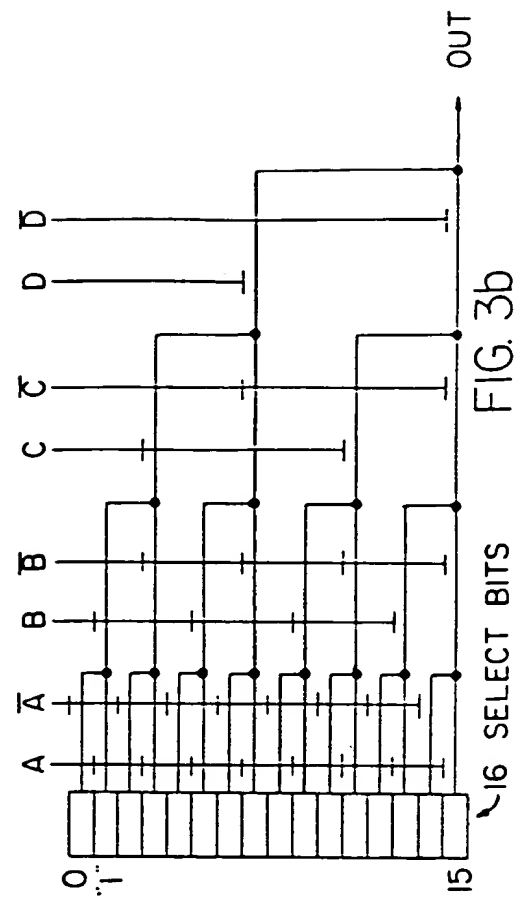
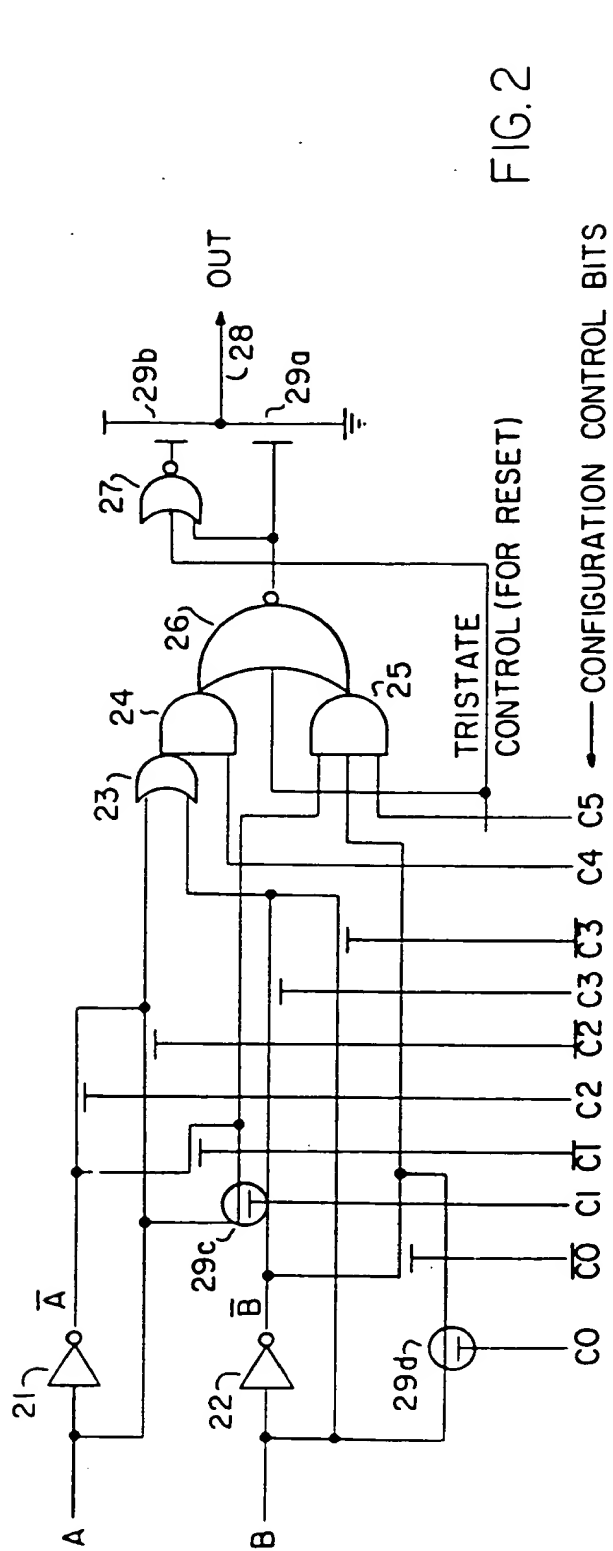
1. A configurable logic array comprising:
 - a plurality of configurable logic elements (CLEs), each CLE having at least one input lead and at least one output lead;
 - a general interconnect structure comprising a plurality of general interconnect leads and a plurality of programmable general interconnect junctions for interconnecting selected ones of the general interconnect leads;
 - one or more access junctions for each input lead for connecting a corresponding general interconnect lead to said input lead;
 - one or more access junctions for each output lead for connecting the output lead to a corresponding general interconnect lead;
 - means for programming the general interconnect junctions and the access junctions such that there is an electrical path connecting a given output lead of a given CLE to a given input lead of a given CLE, the electrical path containing two access junctions and at least a portion of one of the general interconnect leads; and
 - at least one special interconnection circuit which permits a selected output lead of one of the CLEs to be connected to a selected input lead of another CLE, the special interconnection circuit not containing any portion of the leads or any junction in the general interconnect structure.
2. A configurable logic array as claimed in claim 1 comprising:
 - a first, a second, a third and a fourth CLE, the second CLE having a first output lead and a second output lead;
 - a first special interconnection circuit which permits an output signal on the first output lead

of the second CLE to be connected to a selected input lead of the first CLE and which also permits the first output signal to be connected to a selected input lead of the third; and

5 a second special interconnection circuit which permits an output signal on the second output lead of the second CLE to be connected to a selected input lead of the fourth CLE.

3. A configurable logic array as claimed in claim
10 1 or 2 wherein the special interconnection circuit comprises a lead connected to the selected output lead and a pass transistor for each input lead of the selected CLE connected between the lead connected to the selected output lead and the corresponding input lead.





		C			
		D			
A	B				
		0	1	1	0
0	0	0	0	1	1
1	0	1	0	0	0
1	1	0	0	0	0
0	1	0	0	0	0

FIG. 3c

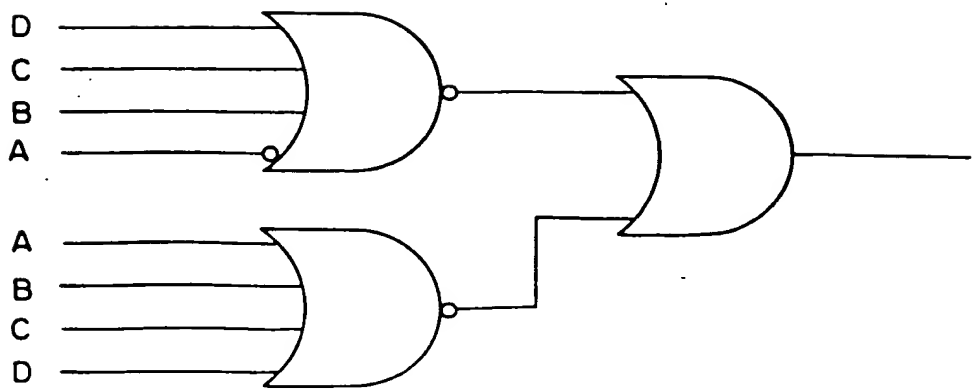


FIG. 3d

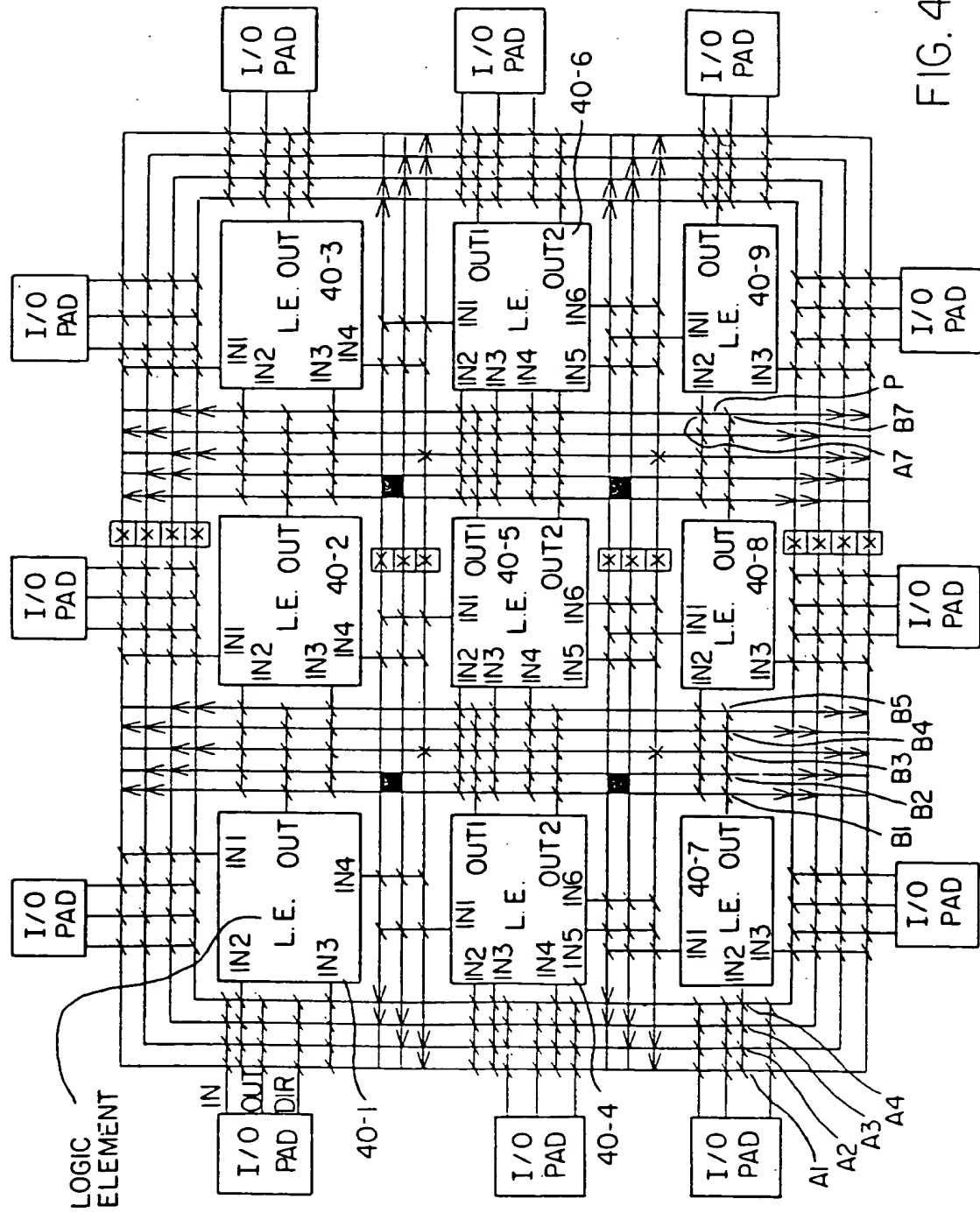


FIG. 4a

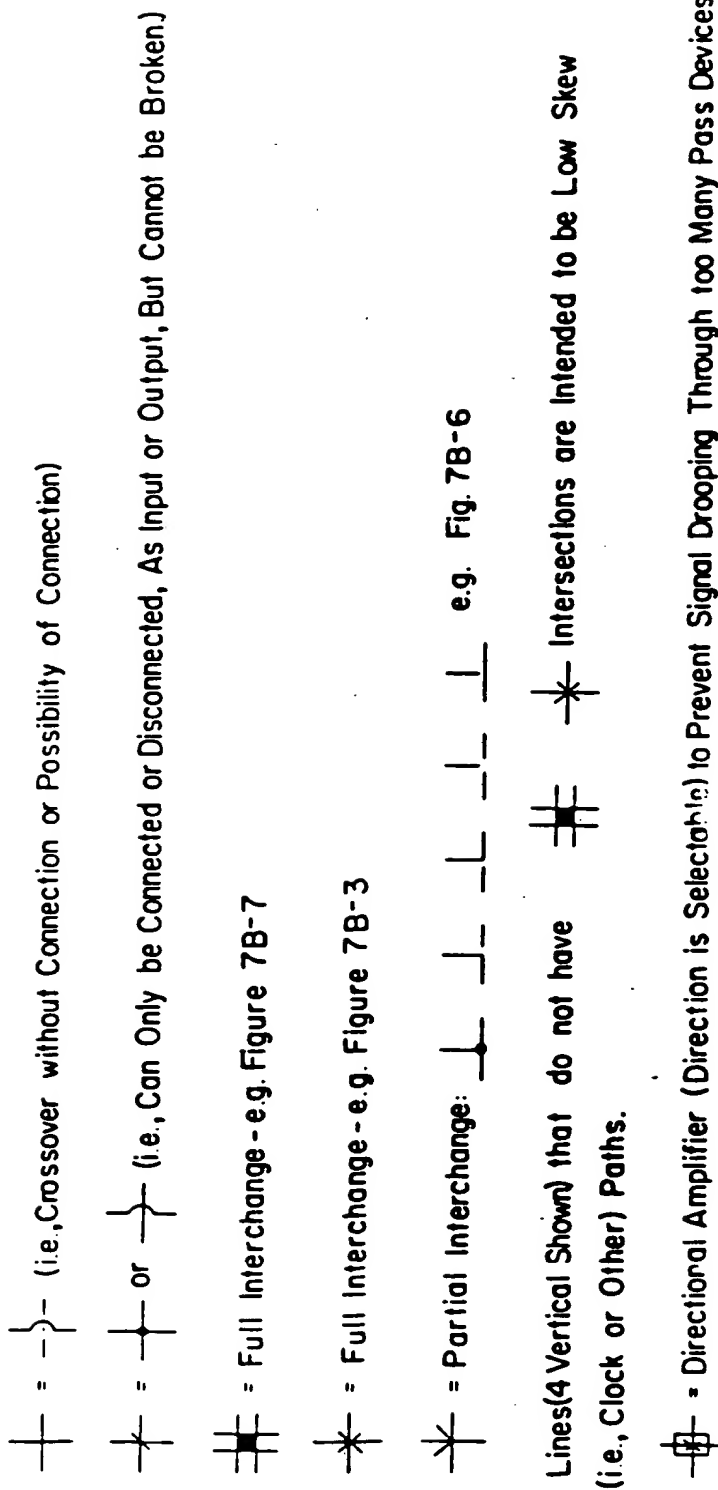


FIG 4b

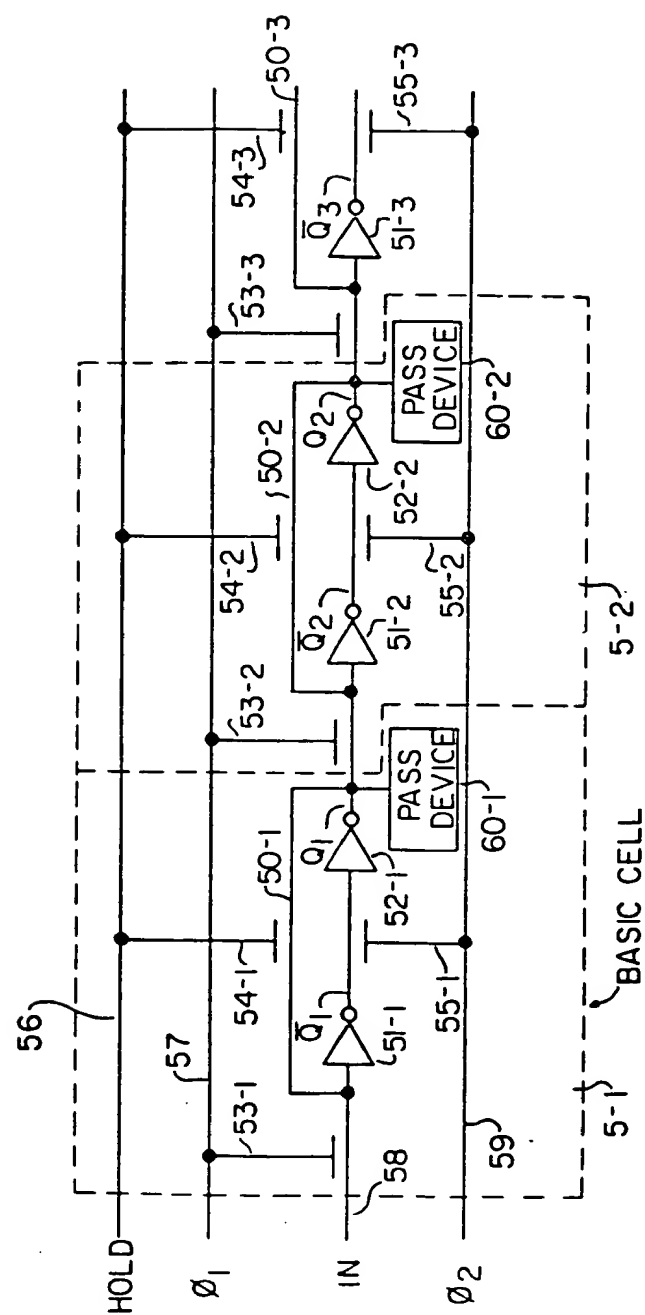
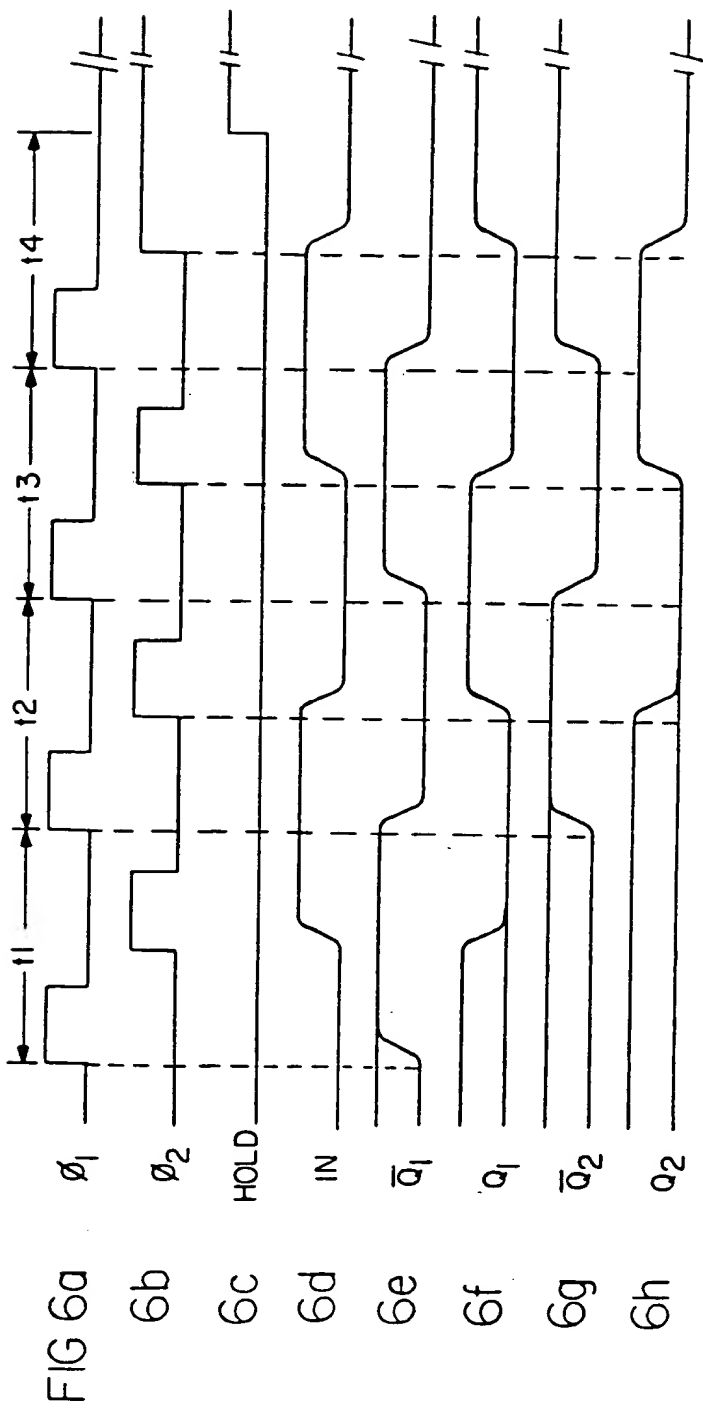
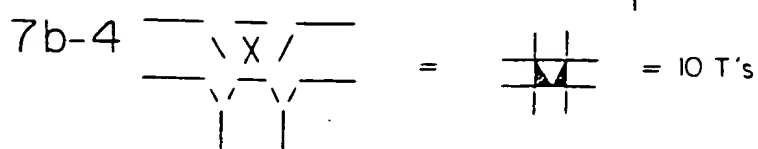


FIG. 5





9/14

$$7b-5 \quad \begin{array}{c} | \\ \times \\ | \end{array} = 5T's = \begin{array}{c} | \\ \diagup \diagdown \\ | \end{array}$$

$$7b-6 \quad \begin{array}{c} \circ \\ | \end{array} = 3T's = \begin{array}{c} \diagup \diagdown \\ | \end{array}$$

20 T interchange

$$7b-7 \quad \begin{array}{c} \# \\ | \end{array}$$

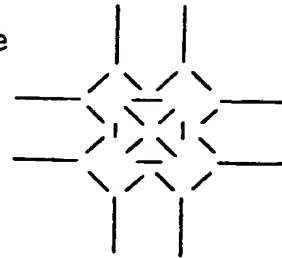
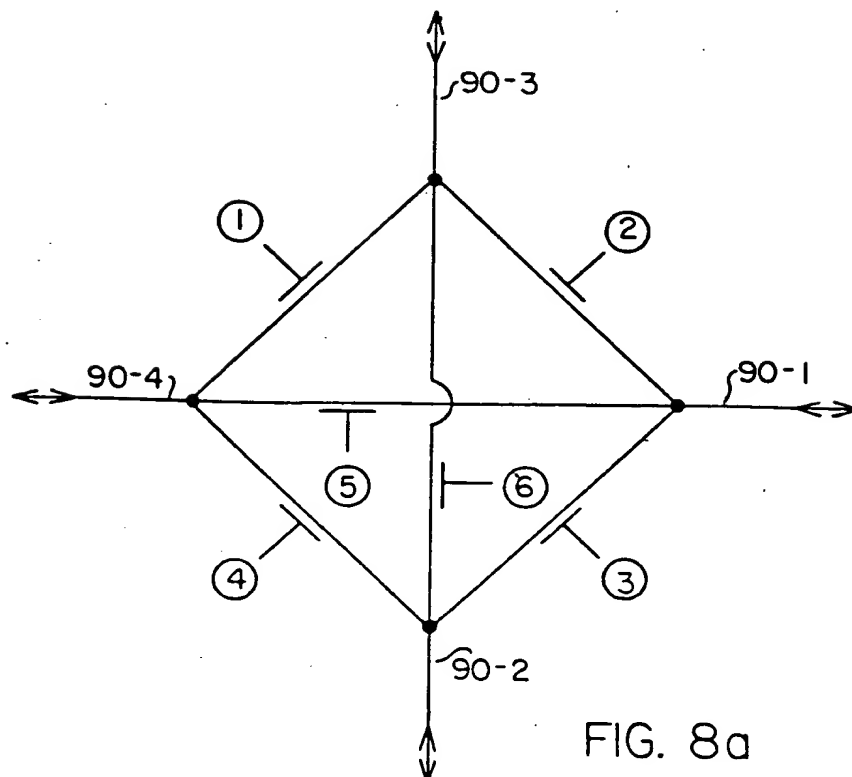


FIG. 7b



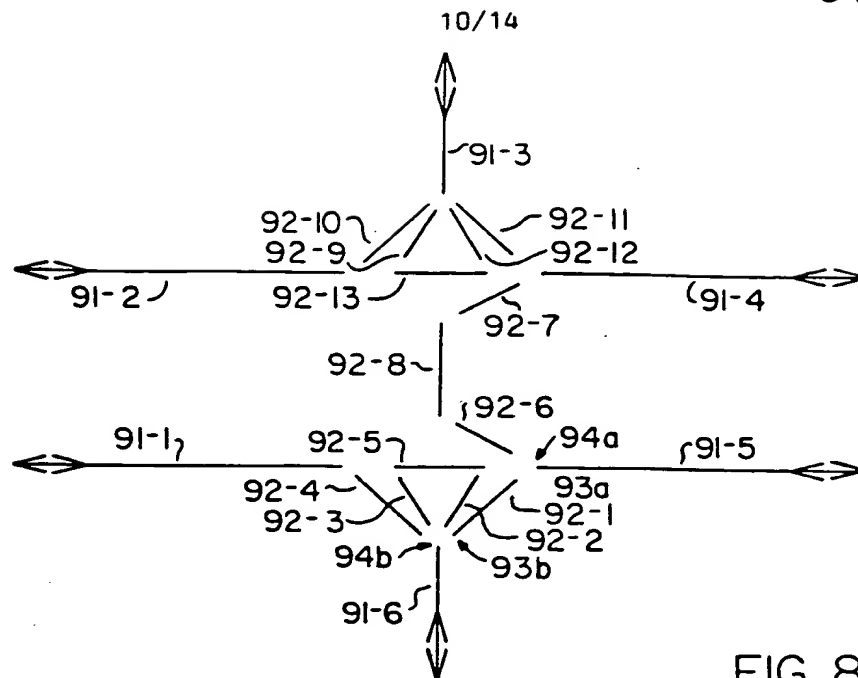


FIG 8b

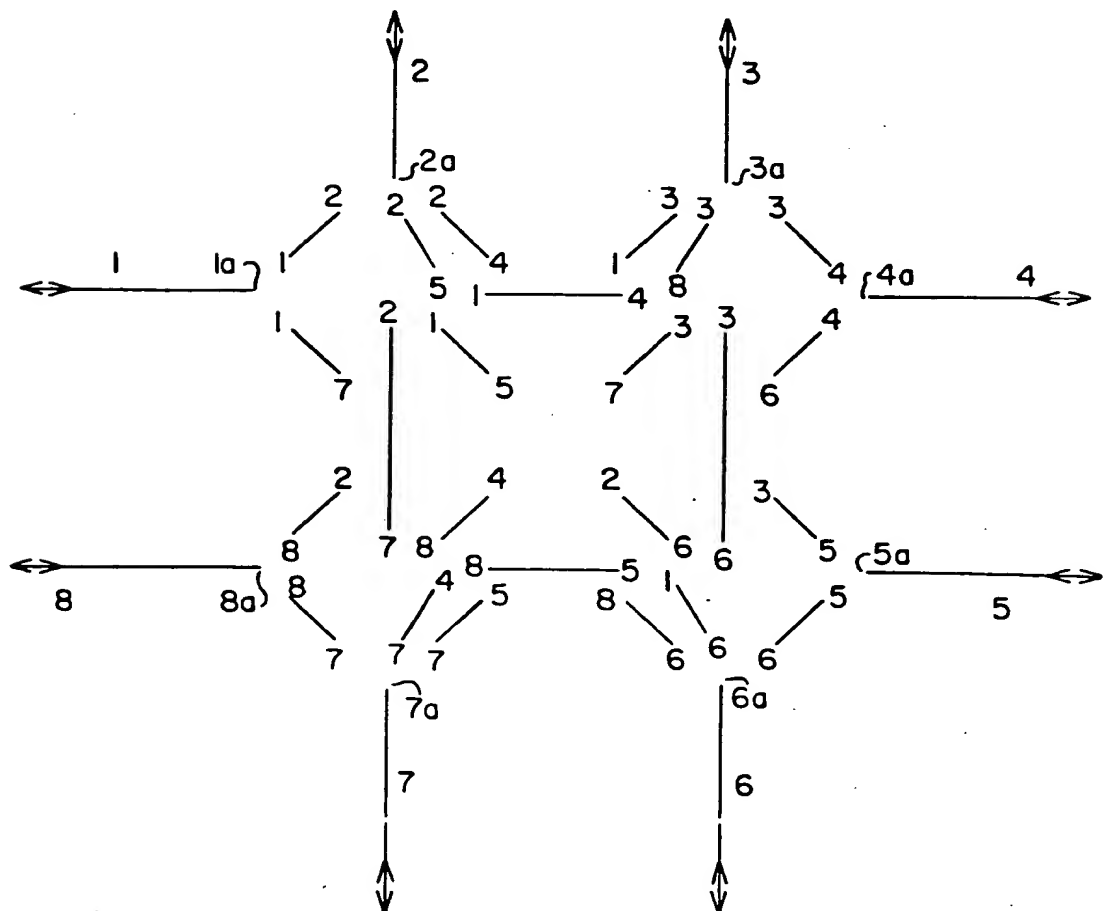


FIG. 8c

Circled numbers on
ends of pass devices
indicate which paths
are directly
connected.

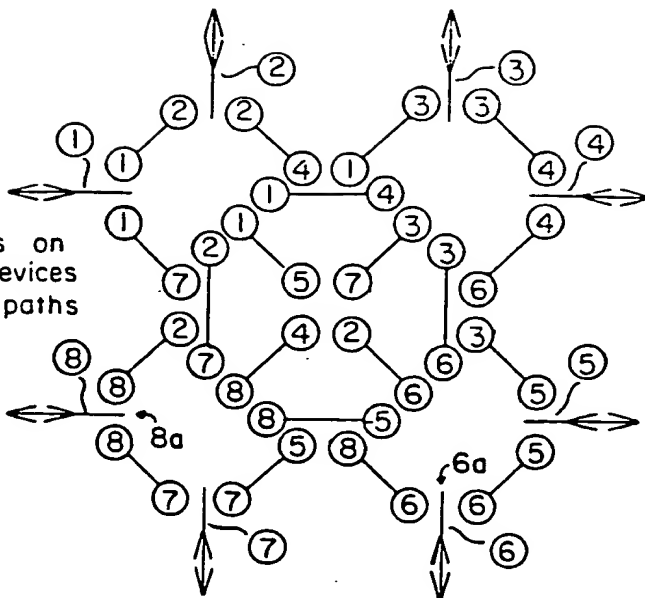
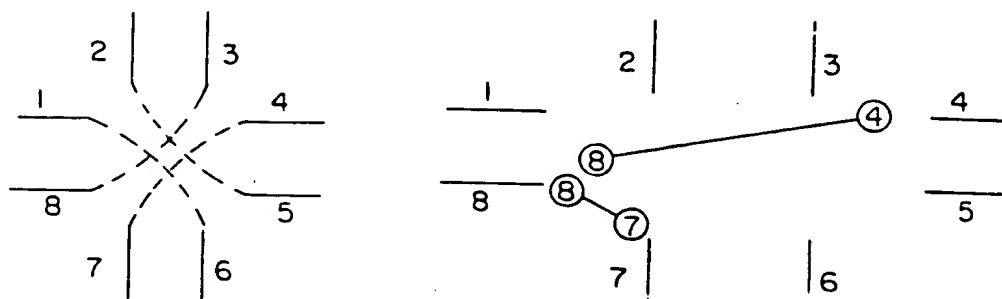
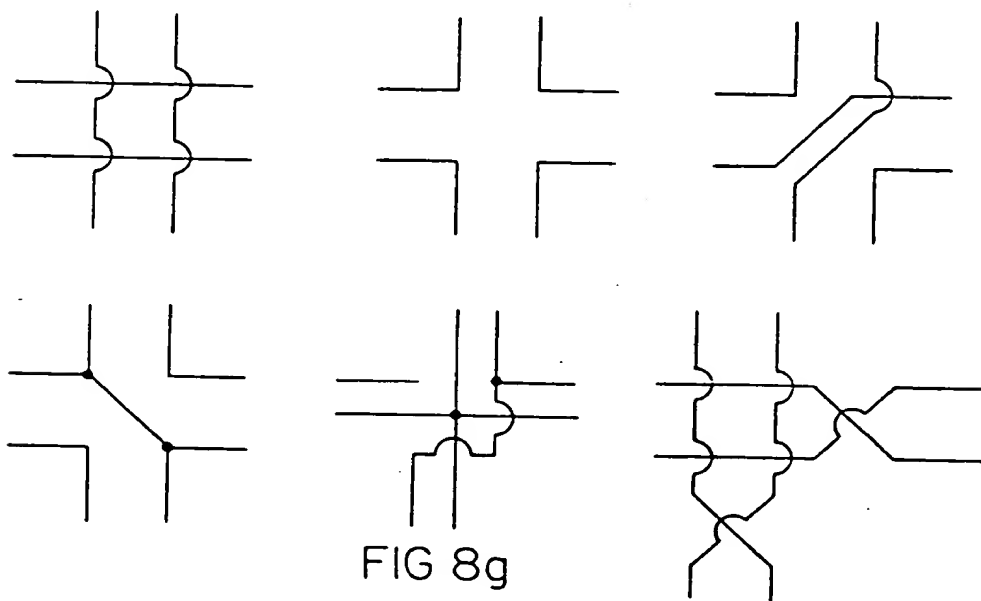
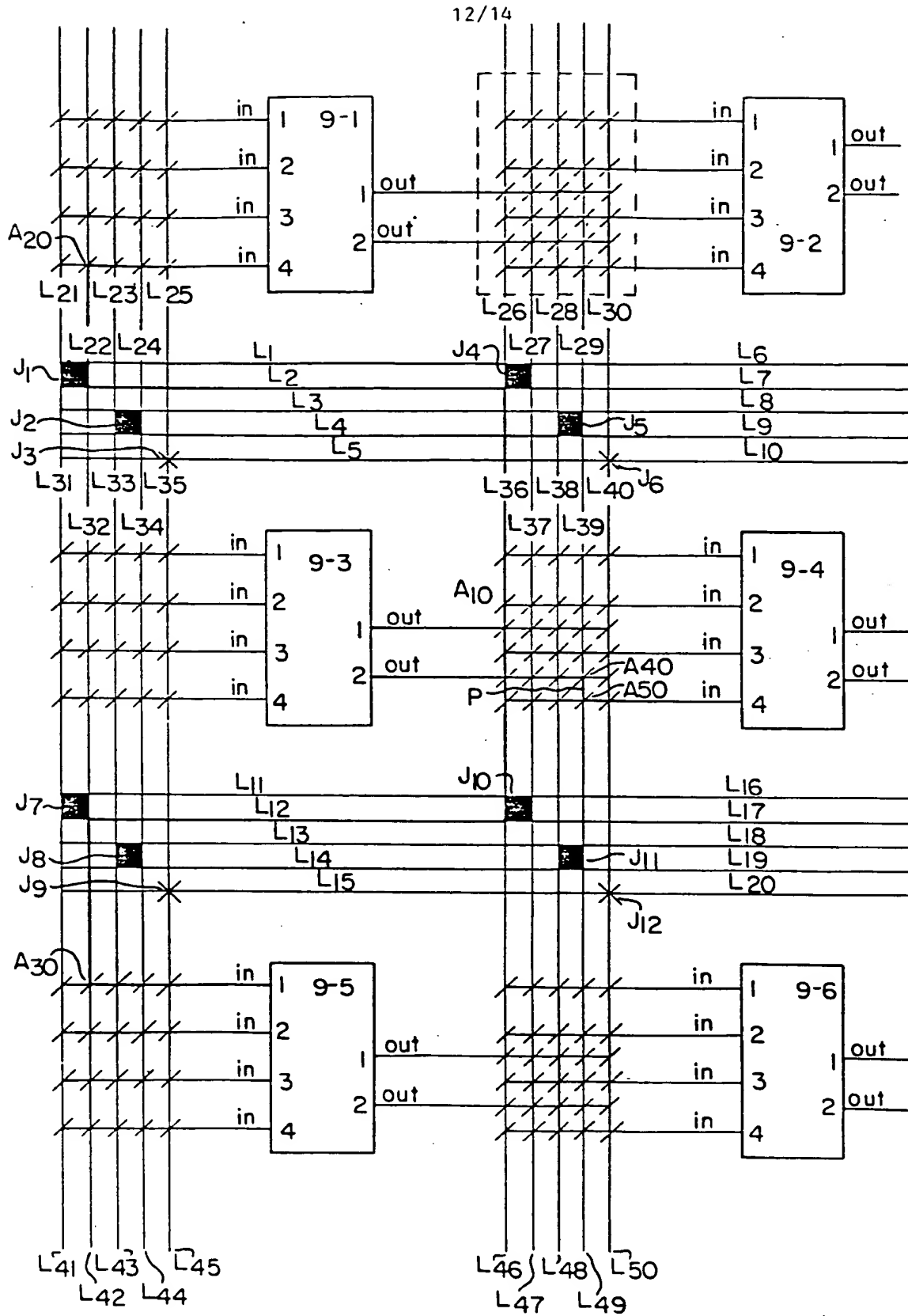


FIG. 8d





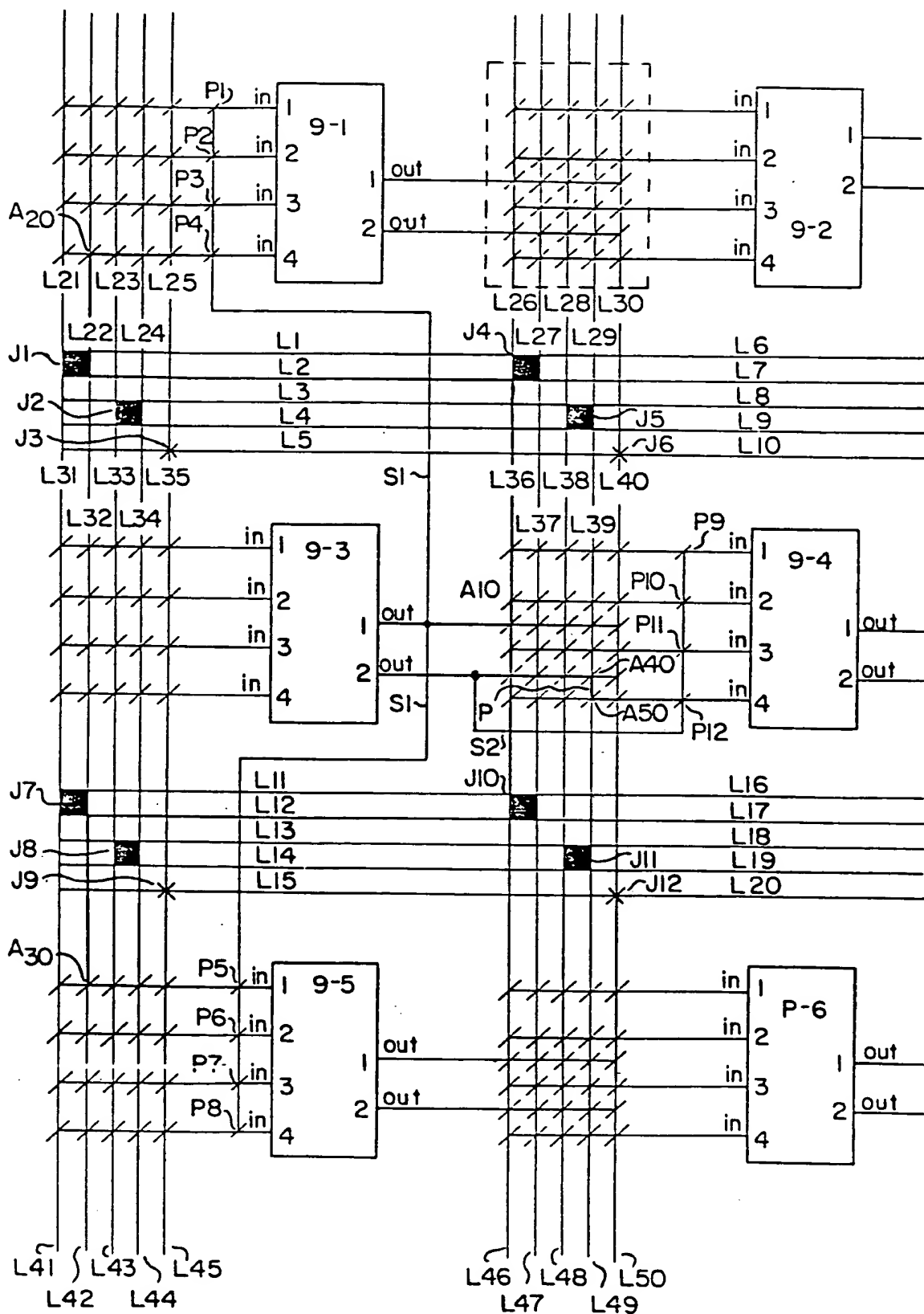


FIG 10

LEAD A	PASS TRANSISTER	LEAD B
91-6	92-1	91-5
91-6	92-2	91-4
91-6	92-3	91-2
91-6	92-4	91-1
91-1	92-5	91-5
91-2	92-6	91-5
91-1	92-7	91-4
91-6	92-8	91-3
91-1	92-9	91-3
91-2	92-10	91-3
91-3	92-11	91-4
91-3	92-12	91-5
91-2	92-13	91-4

FIG.II

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